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# VLSI Implementation of High Bit ALU using Programmable Bidirectional Gate

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**ABSTRACT-** The scaling of devices has two major limitations; one is the size reduction is not feasible beyond particle level and the other one is the reduction of size leading to many second-order effects. In order to make the IC industry to be aligned with Moore's law, a new technology paradigm is essential at this moment. One such possibility is reversible logic based computation of digital systems. Fundamentally, the reversible logic circuits are having one to one mapping between input and output. They are constructed using the reversible gates. In this paper, the two novel 4\*4 reversible logic gates (HNG and PFAG) are used with minimal delay, and may be configured to produce a variety of logical calculations on fixed output lines based on programmable select input lines. The proposed RALU design is verified and its advantages over the only existing ALU design are quantitatively analyzed. The proposed design is synthesized using Xilinx ISE software and simulated using MODEL SIM 6.5b.

**KEYWORDS:** Reversible Gates, Arithmetic Unit (ALU), Garbage Output, Quantum Cost

## I. INTRODUCTION

In modern VLSI system power dissipation is very high due to rapid switching of internal signals. The complexity of VLSI circuits increases with each year due to packing more and more logic elements into smaller volumes. Hence power dissipation has become the main area of concern in VLSI design. Reversible logic has its basics from thermodynamics of information processing. According to this, traditional irreversible circuits generate heat due to the loss of information during computation. In order to avoid this information loss the conventional circuits are modeled using reversible logic. Landauer [1961] showed that the circuits designed using irreversible elements dissipate heat due to the loss of information bits [1]. It is proved that the loss of one bit of information results in dissipation of  $KT \cdot \log_2$  joules of heat energy where K is the Boltzmann constant and T is the temperature at which the operation is performed. Bennett [1973] showed that this heat dissipation due to information loss can be avoided if the circuit is designed using reversible logic gates [2]. A gate is considered to be reversible only if for each and every input there is a unique output assignment. Hence there is a one to one mapping between the input and output vectors. A reversible logic gate is an n-input, n-output device indicating that it has same number of inputs and outputs. A circuit that is built from reversible gates is known as reversible logic circuit. In this paper, we design a 16 bit reversible ALU that can perform eight operations simultaneously. The eight operations include addition, subtraction, AND, NAND, OR, NOR and XOR. All the modules are simulated in modalism SE 6.5 and synthesized using Xilinx ISE 14.1.

## II. REVERSIBLE GATES

Reversible logic is one such possible computing technique in order to overcome the above discussed challenges. In reversible logic, it requires an equal number of inputs and outputs. Reversible computation has the provision to reproduce the input from the output. Conventionally available, the simplest example of reversible computation is 'NOT' gate. It produces logic '0' for the input '1'; by applying this output '0' to the input, it is possible to reproduce the input. So 'NOT' gate is a conventionally available Reversible Gate. So, when the number of inputs and outputs are equal, then there is no heat dissipation according to Landauer's principle (Landauer 1961). A reversible gate consists of an equal number of inputs and number of outputs [3, 4]. The size of the reversible gate is defined by the number



inputs/outputs. The general structure of reversible gate is shown in Figure 1, where  $I_1, I_2, \dots, I_n$  are inputs and  $O_1, O_2, \dots, O_n$  are outputs of the reversible gate. For particular  $i$ , there exists a relation  $I_i \rightarrow O_i$  [5].

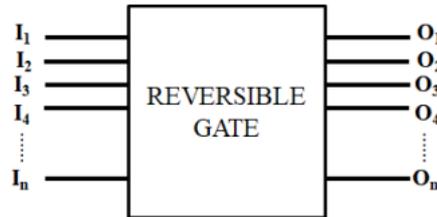


Figure 1: Generic structure of Reversible Gate

The realization of the reversible logic circuits needs to be low power, high speed and beyond Landauer energy limit. One such nanotechnology is Quantum Cellular Automata (QCA); where information is stored in the form of polarity in the small quantum dots. The information processing and propagation in QCA are by means of electrostatic force (Coulomb interaction) between the adjacent dots [6]. Hence, in this Thesis, we are focusing on the Reversible logic based circuit design and its realization in QCA.

o **BASIC REVERSIBLE GATES**

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is shown in Fig. 2. It is the only 2x2 reversible gate available and is commonly used for fan out purposes. Consider the input B as constant. When B is zero, the gate acts as a copying gate or a buffer where both the output lines contain the input A. When B is one, the complement of A is obtained at the output Q. The 3x3 reversible gates include Toffoli gate, Fredkin gate, New gate and Peres gate, all of which can be used to realize various Boolean functions. Fredkin gate is shown in Fig. 3. The 4x4 reversible gates include TSG gate, MKG gate, HNG gate, PFAF gate etc.

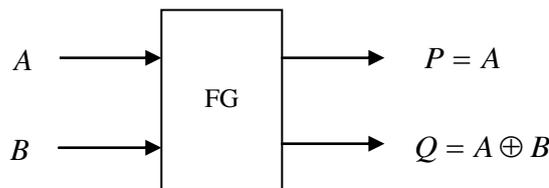


Figure 2: Feynman gate

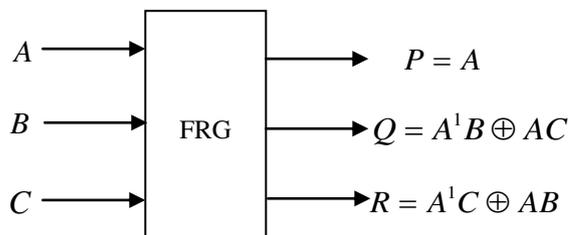


Figure 3: Fredkin gate

Figure 4 shows the Peres gate. Some of the 3x3 gates are designed for implementing some important combinational functions in addition to the basic functions. Most of the above mentioned gates can be used in the design of reversible adders.

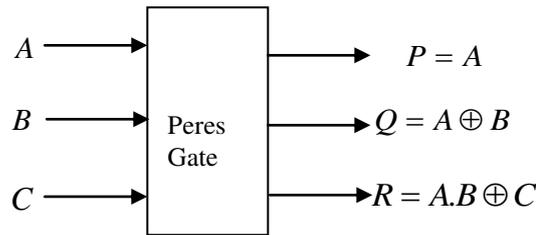


Figure 4: Peres gate

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. The HNG gate, presented in [10], produces the following logical output calculations:

$$P = A \tag{1}$$

$$Q = B \tag{2}$$

$$R = A \oplus B \oplus C \tag{3}$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \tag{4}$$

The quantum cost and delay of the HNG is 6. When  $D = 0$ , the logical calculations produced on the  $R$  and  $S$  outputs are the required sum and carry-out operations for a full adder. The block diagram representation of the HNG is presented in Fig. 5.

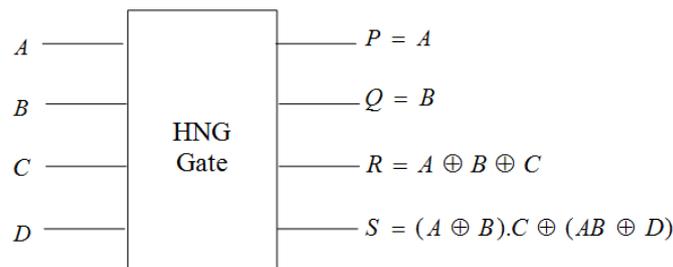


Figure 5: HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or (PFAG) gate – is presented which produces outputs

$$P = A \tag{5}$$

$$Q = A \oplus B \tag{6}$$

$$R = A \oplus B \oplus C \tag{7}$$

$$S = (A \oplus B)C \oplus AB \oplus D \tag{8}$$

Figure 6 shows the block diagram of the PFAG gate. This gate is an extension of the Peres gate for ALU realization.

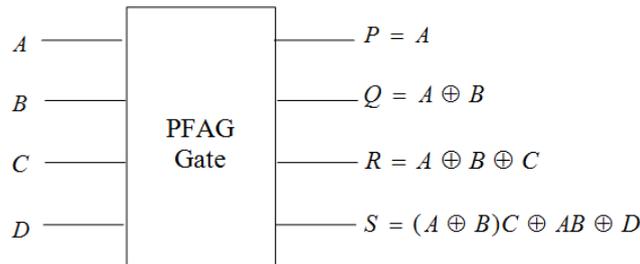


Figure 6: PFAG Gate

### III. REVERSIBLE ALU DESIGN

ALU works as a data processing components which is an important part in the central process unit (CPU). Besides, it is the main performer in any computing devices. ALU is a multi-functional circuit that performs one of a few possible functions on two operands of A and B which is depending on the control inputs.

The S2, S1 and S0 are the selection lines while Cin is the input carry. Input A and B are the data input for the ALU design. Based on the truth table shown in Table 1, when selection line S2 is equal to zero, the circuit performs eight arithmetic operations and when selection line S2 is equal to one, the circuit performs the logic operations of OR, EX-OR, AND and NOT functions.

Table 1: Function table of ALU

S2	S1	S0	Cin	Operation	Function
0	0	0	0	F=A	Transfer A
0	0	0	1	F=A+1	Increment A
0	0	1	0	F=A+B	Addition
0	0	1	1	F=A+B+1	Add with carry
0	1	0	0	F=A+B'	Subtract with borrow
0	1	0	1	F=A+B'+1	Subtraction
0	1	1	0	F=A-1	Decrement A
0	1	1	1	F=A	NAND
1	0	0	0	F=A^B	OR
1	0	0	1	F=A⊕B	EX-OR
1	0	1	0	F=A&B	AND
1	0	1	1	F=A'	NOT

The proposed reversible ALU is designed to produce the same function as implemented by conventional ALU. Figure 7 is the block diagram of proposed reversible ALU designs. It has two main logic circuit design, namely, control unit and reversible full adder and the proposed design has five constants signals (e.g: Cinput1, Cinput2, Cinput3, Cinput4 and Cinput5) with a provision for realizing the eight arithmetic operations and four logic operations.

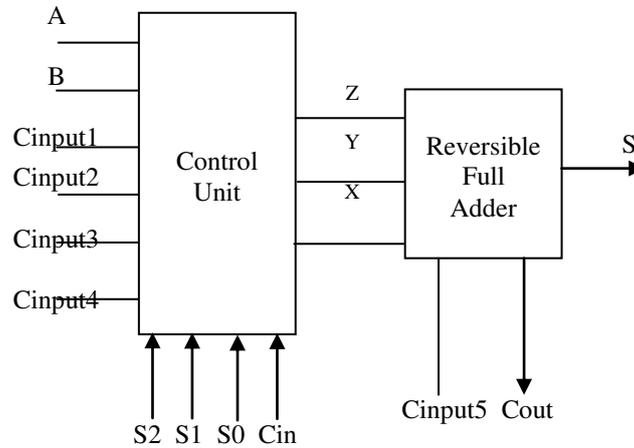


Figure 7: Block Diagram of RALU Design

(i) Control Unit

Control unit is a critical part in the reversible ALU design. Control unit performs the arithmetic operations inside the ALU. As shown in Fig.8, the proposed control unit design is made up from three Feynman gates, three R-I gates and one Fredkin gate. Four control variables  $S_2$ ,  $S_1$ ,  $S_0$  and  $C_{in}$  select twelve different operations in the reversible ALU design. The arithmetic and logic operations are differentiated using the variable input of  $S_2$ . The control unit has four constant signals. There are eight garbage outputs in the proposed control unit logic circuit.

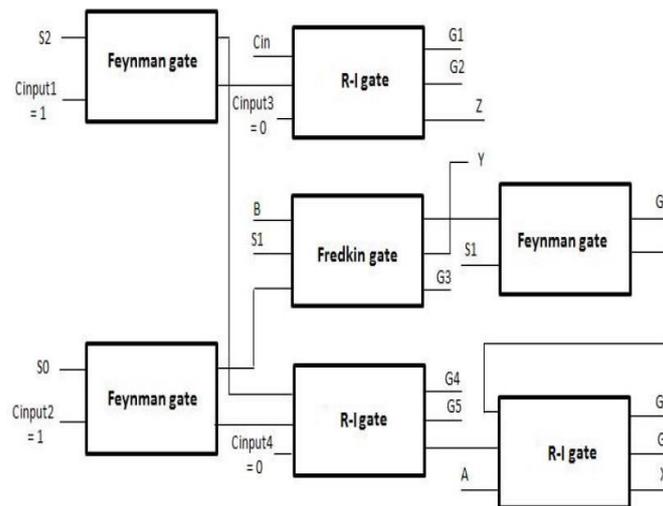


Figure 8: Block diagram of control unit

IV. SIMULATION RESULTS

In the figure 9 and figure 10 show the view technology schematic and resistor transfer level of 32-bit RALU based on HNG, input of the Reversible Arithmetic logic unit (RALU) is represented by  $A_1$ ,  $B_1$ , previous carry of the RALU is represented by  $C_{in1}$ , select line of the RALU is represented by  $S_{11}$ ,  $S_{12}$  and  $S_{13}$  and output of the RALU is represented by result respectively.

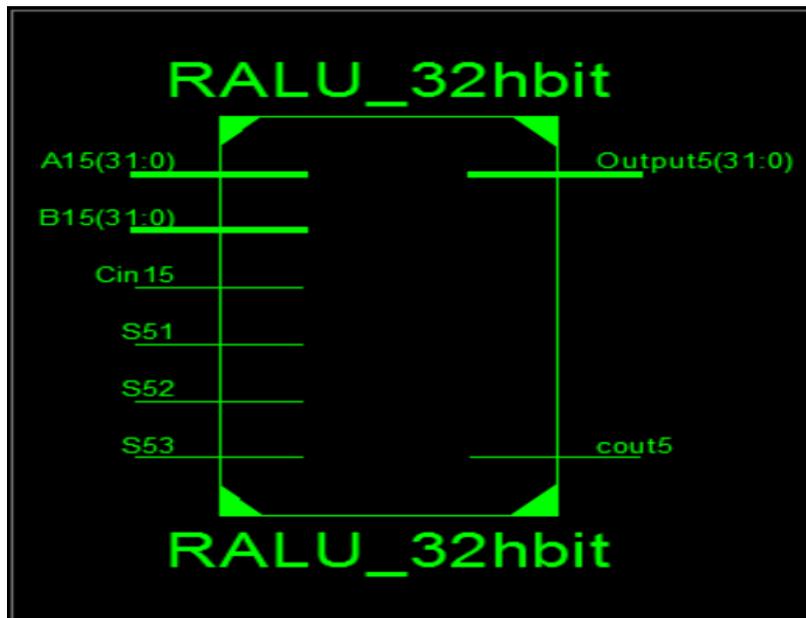


Figure 9: View Technology Schematic for 32-bit RALU

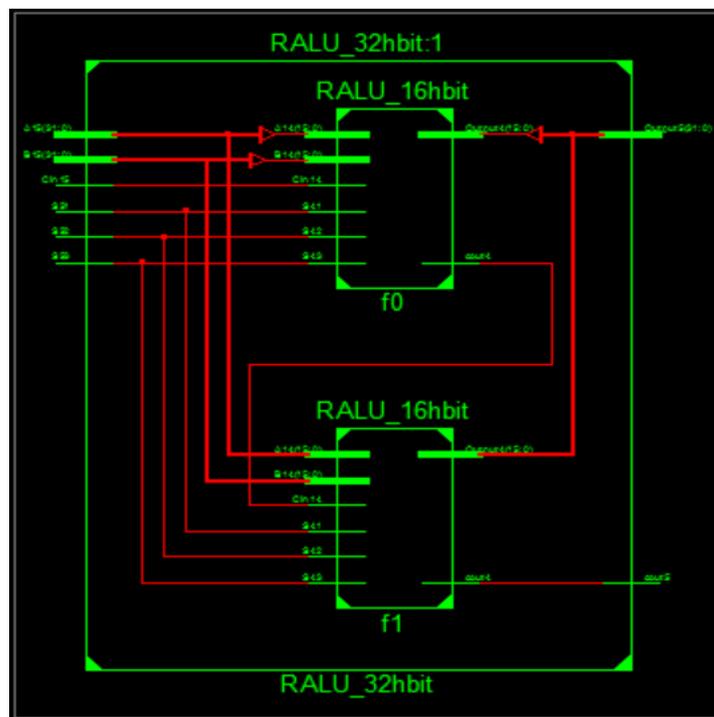


Figure 10: RTL View for 32-bit RALU

Table 2: Proposed Design based on HNG Gate

parameter	LUTs	FF	IOBS	Delay
1-bit	2	2	8	1.044
2-bit	7	7	11	2.435
4-bit	8	8	16	3.478



8-bit	25	25	29	5.790
16-bit	49	49	53	10.440
32-bit	97	97	101	19.695
64-bit	193	193	197	38.205
128-bit	385	385	389	75.224
256-bit	769	769	773	140.260
512-bit	1537	1537	1541	297.261

### V. CONCLUSION

In this paper, the reversible ALU design is proposed with two unique design paradigms. The proposed reversible ALU designs are verified using Xilinx software. Both proposed designs are analyzed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. The simulation results illustrate that the proposed reversible ALU design 2 outperforms the proposed reversible ALU design 1 and conventional ALU design.

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